CLAIMS

1. A method of forming a memory cell for a memory cell array; said method comprising:

forming at least two deep trench structures in a semiconductor substrate, at least one of said deep trench structures being in electrical contact with a buried strap region formed in said substrate that adjoins said at least one deep trench structure; and

patterning and etching said semiconductor substrate to form at least one isolation trench that adjoins said two deep trenches, said patterning using a mask comprised of a continuous lines and spaces pattern such that at least one active area is defined by said isolation trench and by said two deep trenches, said active area including said buried strap region, each of said lines and said spaces extending across an entire length of said memory cell array.

2. The method of claim 1 wherein said at least two deep trench structures are separated by a distance 3F, where F is a minimum feature size.

3. The method of claim 1 wherein said step of forming at least one deep trench structure comprises:

forming a deep trench within a semiconductor substrate;

forming said buried plate region adjoining a bottom region of said deep trench within said semiconductor substrate;

forming a dielectric film along sidewalls of the deep trench;

patterning a masking layer such that a portion of said dielectric film is covered by said masking layer and a remaining portion of said dielectric film is exposed;

removing an upper region of said exposed portion of said dielectric film such that a trench collar is formed along an upper portion of a side of said deep trench; and

partly filling said deep trench with doped polysilicon, the dopants in the polysilicon diffusing through

said side of said deep trench into adjoining regions of said semiconductor substrate during subsequent thermal processing steps to form said buried strap region along said side of said deep trench.

4. The method of claim 3 wherein said openings in said masking layer have a pitch equal to 2F, where F is minimum feature size in said memory cell, said openings in said masking layer exposing a common region of said dielectric film in each of said plurality of said memory cells, said buried strap region of each of said plurality of said memory cells adjoining a same side of the deep trenches.

5. The method of claim 3 wherein said openings in said masking layer have a pitch equal to 4F, where F is a minimum feature size of said memory cell, said openings in said masking layer exposing opposing regions of said dielectric film in adjacent ones of said plurality of said memory cells, said buried strap region of said adjacent ones of said plurality of said memory cells adjoining opposite sides of its deep trenches.

6. The method of claim 3 further comprising:

forming a trench top oxide layer atop said doped polysilicon of said at least one deep trench;

forming a gate dielectric layer on said side of said deep trench;

filling said deep trench with a further polysilicon layer atop said trench top oxide layer;

forming a doped region in a top surface of said semiconductor substrate adjacent to said gate dielectric layer;

forming a contact region to said further polysilicon layer that connects said further polysilicon layer to a word line; and

forming another contact region to said doped region that connects said doped region to a bit line.

7. A memory cell for a memory cell array comprised of a plurality of said memory cells arranged in rows and columns; said memory cell comprising:

at least two deep trench structures formed in a semiconductor substrate, at least one of said deep trench structures being in electrical contact with a buried strap region formed in said substrate that adjoins said at least one deep trench structure; and

at least one isolation trench adjoining said two deep trench structures, said one isolation trench being defined using a mask comprised of a lines and spaces pattern such that at least one active area is defined by said isolation trench and by said two deep trenches, said active area including said buried strap region, each of said lines and said spaces extending across said memory cell array.

8. The memory cell of claim 7 wherein said at least two deep trench structures are separated by a distance 3F, where F is a minimum feature size.

9. The memory cell of claim 7 wherein said at least one deep trench structure comprises:

a deep trench formed within a semiconductor substrate;

a buried plate region adjoining a bottom region of said at least one deep trench within said semiconductor substrate;

a dielectric film formed along sidewalls of the deep trench, an upper region of a portion of said dielectric film being removed such that a trench collar is formed along a middle portion of a side of said deep trench, said portion of said dielectric film being defined by a patterned masking layer such that a further portion of said dielectric film is covered by said masking layer and said portion of said dielectric film is exposed;

said deep trench being at least partly filled with doped polysilicon, the dopants in the polysilicon diffusing through said side of said deep trench into an adjoining region

of said semiconductor substrate to form said buried strap region along said side of said deep trench.

10. The memory cell of claim 9 wherein openings in said masking layer have a pitch equal to twice a minimum feature size in said memory cell, said openings in said masking layer exposing a common region of said dielectric film in each of said plurality of said memory cells, said buried strap region of each of said plurality of said memory cells adjoining a same side of the deep trenches.

11. The memory cell of claim 9 wherein openings in said masking layer have a pitch equal to four times that of a minimum feature size of said memory cell, said openings in said masking layer exposing opposing regions of said dielectric film in adjacent ones of said plurality of said memory cells, said buried strap region of said adjacent ones of said plurality of said memory cells adjoining opposite sides of its deep trenches.

12. The memory cell of claim 9 further comprising:

a trench top oxide layer formed atop said doped polysilicon in said at least one deep trench;

a gate dielectric layer formed on said side of said deep trench;

said deep trench being filled with a further polysilicon layer atop said trench top oxide layer;

a doped region formed in a top surface of the semiconductor substrate adjacent to said gate dielectric layer;

a contact region to said further polysilicon layer that connects said further polysilicon layer to a word line; and

another contact region to said doped region that connects said doped region to a bit line.

13. A method of forming a buried strap region in a memory cell of a memory cell array; said method comprising:

forming a deep trench within a semiconductor substrate;

forming a dielectric film along sidewalls of the deep trench;

patterning a masking layer such that a portion of said dielectric film is covered by said masking layer and a remaining portion of said dielectric film is exposed;

removing an upper region of said exposed portion of said dielectric film such that a trench collar is formed along an upper portion of a side of said deep trench; and

filling said deep trench partly with doped polysilicon, the dopants in the polysilicon diffusing through said side of said deep trench into adjoining regions of said semiconductor substrate during subsequent thermal processing steps to form said buried strap region along said side of said deep trench.

14. The method of claim 13 wherein said openings in said masking layer have a pitch equal to 2F, where F is a minimum feature size in said memory cell, said openings in said masking layer exposing a common region of said dielectric film in each of said plurality of said memory cells, said buried strap region of each of said plurality of said memory cells adjoining a same side of the deep trenches.

15. The method of claim 13 wherein said openings in said masking layer have a pitch equal to 4F, where F is a minimum feature size of said memory cell, said openings in said masking layer exposing opposing regions of said dielectric film in adjacent ones of said plurality of said memory cells, said buried strap region of said adjacent ones of said plurality of said memory cells adjoining opposite sides of its deep trenches.

16. The method of claim 13 further comprising:

patterning and etching said semiconductor substrate to form at least one isolation trench that adjoins said deep trench, said patterning using a mask comprised of a lines and spaces pattern such that at least one active area is defined by said isolation trench, by said deep trench and by an

adjacent deep trench; each of said lines and said spaces extending across said memory cell array;

forming a trench top oxide layer atop said doped polysilicon;

forming a gate dielectric layer on said side of said deep trench;

filling said deep trench with a further polysilicon layer atop said trench top oxide layer;

forming a doped region in a top surface of the semiconductor substrate adjacent to said gate dielectric layer;

forming a contact region to said further polysilicon layer and connecting said further polysilicon layer to a word line; and

forming another contact region to said doped region and connecting said doped region to a bit line.

17. A buried strap forming structure within a memory cell of a memory cell array; said region comprising:

a deep trench formed within a semiconductor substrate;

a dielectric film formed along sidewalls of the deep trench, an upper region of a portion of said dielectric film being removed such that a trench collar is formed along an upper portion of one side of said deep trench, said portion of said dielectric film being defined by a patterned masking layer such that a further portion of said dielectric film is covered by said masking layer and said portion of said dielectric film is exposed; and

doped polysilicon at least partly filling said deep trench, the dopants in the polysilicon diffusing through said one side of said deep trench into an adjoining region of said semiconductor substrate to form a buried strap region along said one side of said deep trench.

18. The buried strap forming structure of claim 17 wherein openings in said masking layer have a pitch equal to 2F, where F is a minimum feature size in said memory cell,

said openings in said masking layer exposing a common region of said dielectric film in each of said plurality of said memory cells, said buried strap region of each of said plurality of said memory cells adjoining a same side of the deep trenches.

19. The buried strap forming structure of claim 17 wherein openings in said masking layer have a pitch equal to 4F, where F is a minimum feature size of said memory cell, said openings in said masking layer exposing opposing regions of said dielectric film in adjacent ones of said plurality of said memory cells, said buried strap region of said adjacent ones of said plurality of said memory cells adjoining opposite sides of its deep trenches.

20. The buried strap forming structure of claim 17 further comprising:

at least one isolation trench that adjoins said deep trench, said isolation trench being patterned using a mask comprised of a lines and spaces pattern such that at least one active area is defined by said isolation trench, said deep trench, and an adjoining trench; each of said lines and said spaces extending across said memory cell array;

a trench top oxide layer disposed atop said doped polysilicon;

a gate dielectric layer formed on said side of said deep trench;

a further polysilicon layer formed atop said trench top oxide layer and filling said deep trench;

a doped region formed in a top surface of the semiconductor substrate adjacent to said gate dielectric layer;

a contact region to said further polysilicon layer connecting said further polysilicon layer to a word line; and

another contact region to said doped region connecting said doped region to a bit line.

21. A method of forming a contact structure to a first terminal of a vertical transistor formed in a

semiconductor substrate; said first terminal being disposed in a surface of said semiconductor substrate adjacent to one side of a deep trench formed in said semiconductor substrate; said vertical transistor further having a gate insulator located along an upper portion of said one side of said deep trench with a top end located adjacent to said first terminal, a gate contact region filling said upper portion of said deep trench, and a further terminal comprising a buried strap region formed along said one side of said deep trench at a bottom end of said gate insulator; said gate contact region being electrically connected to an insulated electrode formed atop said semiconductor substrate; a further side of said deep trench being insulated from said semiconductor substrate by an insulating film; said method comprising:

forming a first insulator layer atop said surface of said semiconductor substrate, said first insulator layer extending up to a top surface of said insulated electrode;

depositing a further insulator layer atop said first insulator layer and atop said insulated electrode;

patterning and etching said further insulator layer and said first insulator layer to form at least one first opening therein that extends down to said first terminal, a remaining portion of said first insulator layer covering said further side of said deep trench;

patterning and etching said further insulator layer to form at least one further opening therein that extends from a top surface of said further insulator layer down to said first opening; and

filling said first opening and said further opening with a conducting material.

22. The method of claim 21 wherein said step of forming said first insulator layer comprises depositing said first insulator layer atop said surface of said semiconductor substrate, and then planarizing said first insulator layer to said top surface of said insulated electrode.

23. The method of claim 21 wherein said first insulator layer comprises a doped glass layer.

24. The method of claim 21 wherein said further insulator layer comprises an oxide material.

25. The method of claim 21 wherein said step of patterning and etching said further insulator layer to form said at least one further opening leaves a region of said further insulator layer atop said remaining portion of said first insulator layer and atop at least part of said insulated electrode.

26. The method of claim 21 wherein said conducting material comprises a metal layer.

27. A method of forming a bit line contact structure to a memory cell of a memory cell array, said memory cell including a vertical transistor and a storage capacitor; said vertical transistor having a first terminal disposed in a surface of a semiconductor substrate adjacent to one side of a deep trench formed in the semiconductor substrate, a gate insulator located along an upper portion of said one side of said deep trench with a top end located adjacent to said first terminal, a gate contact region filling said upper portion of said deep trench, and a further terminal comprising a buried strap region formed along said one side of said deep trench at a bottom end of said gate insulator; said storage capacitor having a buried plate formed in said semiconductor substrate and a further plate formed in said deep trench and electrically coupled to said buried strap region; said gate contact region being electrically connected to an insulated word line formed atop said semiconductor substrate; a further side of said deep trench being insulated from said semiconductor substrate by an insulating film; said method comprising:

forming a first insulator layer atop said surface of said semiconductor substrate, said first insulator layer extending up to a top surface of said insulated word line;

depositing a further insulator layer atop said first insulator layer and atop said insulated word line;

patterning and etching said further insulator layer and said first insulator layer to form at least one first opening therein that extends down to said first terminal, a remaining portion of said first insulator layer covering said further side of said deep trench;

patterning and etching said further insulator layer to form at least one further opening therein that extends from a top surface of said further insulator layer down to said first opening; and

filling said first opening and said further opening with a conducting material.

28. The method of claim 27 wherein said step of forming said first insulator layer comprises depositing said first insulator layer atop said surface of said semiconductor substrate, and then planarizing said first insulator layer to said top surface of said insulated word line.

29. The method of claim 27 wherein said first insulator layer comprises a doped glass layer.

30. The method of claim 27 wherein said further insulator layer comprises an oxide material.

31. The method of claim 27 wherein said step of patterning and etching said further insulator layer to form said at least one further opening leaves a region of said further insulator layer atop said remaining portion of said first insulator layer and atop at least part of said insulated word line.

32. The method of claim 27 wherein said conducting material comprises a metal layer.

33. A contact structure to a first terminal of a vertical transistor formed in a semiconductor substrate; said first terminal being disposed in a surface of said semiconductor substrate adjacent to one side of a deep trench formed in said semiconductor substrate; said vertical transistor further having a gate insulator located along an upper portion of said one side of said deep trench with a top end located adjacent to said first terminal, a gate contact

region filling said upper portion of said deep trench, and a further terminal comprising a buried strap region formed along said one side of said deep trench at a bottom end of said gate insulator; said gate contact region being electrically connected to an insulated electrode formed atop said semiconductor substrate; a further side of said deep trench being insulated from said semiconductor substrate by an insulating film; said contact structure comprising:

a first insulator layer disposed atop said surface of said semiconductor substrate, said first insulator layer having a top surface substantially coplanar with a top surface of said insulated electrode;

a further insulator layer disposed atop said first insulator layer and atop said insulated electrode;

at least one first opening being formed in said further insulator layer and said first insulator layer that extends from within said further insulator layer through said first insulator layer down to said first terminal, a remaining portion of said first insulator layer covering said further side of said deep trench;

at least one further opening being formed within said further insulator layer from a top surface of said further insulator layer to said first opening; and

a conducting material filling said first opening and said further opening.

34. The contact structure of claim 33 wherein said first insulator layer comprises a doped glass layer.

35. The contact structure of claim 33 wherein said further insulator layer comprises an oxide material.

36. The contact structure of claim 33 wherein a region of said further insulator layer remains atop said remaining portion of said first insulator layer and at least part of said insulated electrode.

37. The contact structure of claim 33 wherein said conducting material comprises a metal layer.

38. A bit line contact structure to a memory cell of a memory cell array, said memory cell including a vertical transistor and a storage capacitor; said vertical transistor having a first terminal disposed in a surface of a semiconductor substrate adjacent to one side of a deep trench formed in said semiconductor substrate, a gate insulator located along an upper portion of said one side of said deep trench with a top end located adjacent to said first terminal, a gate contact region filling said upper portion of said deep trench, and a further terminal comprising a buried strap region formed along said one side of said deep trench at a bottom end of said gate insulator; said storage capacitor having a buried plate formed in said semiconductor substrate and a further plate formed in said deep trench and electrically coupled to said buried strap region; said gate contact region being electrically connected to an insulated word line formed atop said semiconductor substrate; a further side of said deep trench being insulated from said semiconductor substrate by an insulating film; said contact structure comprising:

a first insulator layer disposed atop said surface of said semiconductor substrate, said first insulator layer having a top surface substantially coplanar with a top surface of said insulated word line;

a further insulator layer disposed atop said first insulator layer and atop said insulated word line;

at least one first opening being formed in said further insulator layer and said first insulator layer that extends from within said further insulator layer through said first insulator layer down to said first terminal, a remaining portion of said first insulator layer covering said further side of said deep trench;

at least one further opening being formed within said further insulator layer from a top surface of said further insulator layer to said first opening; and

a conducting material filling said first opening and said further opening.

39. The bit line contact structure of claim 38 wherein said first insulator layer comprises a doped glass layer.

40. The bit line contact structure of claim 38 wherein said further insulator layer comprises an oxide material.

41. The bit line contact structure of claim 38 wherein a region of said further insulator layer remains atop said remaining portion of said first insulator layer and at least part of said insulated word line structure.

42. The bit line contact structure of claim 38 wherein said conducting material comprises a metal layer.

43. A method of forming a memory cell for a memory cell array; said method comprising:

forming at least two deep trenches within a semiconductor substrate;

forming a buried plate region adjoining a bottom region of at least one of said two deep trenches within said semiconductor substrate;

forming a dielectric film along sidewalls of said at least one deep trench;

patterning a masking layer such that a portion of said dielectric film is covered by said masking layer and a remaining portion of said dielectric film is exposed;

removing an upper region of said exposed portion of said dielectric film such that a trench collar is formed along an upper portion of a side of said at least one deep trench;

partly filling said at least one deep trench with doped polysilicon, the dopants in the polysilicon diffusing through said side of said at least one deep trench into an adjoining region of said semiconductor substrate during subsequent thermal processing steps to form a buried strap region along said side of said deep trench;

forming a trench top oxide layer atop said doped polysilicon;

forming a gate dielectric layer on said upper portion of said side of said at least one deep trench;

filling said at least one deep trench with a further polysilicon layer atop said trench top oxide layer;

patterning and etching said semiconductor substrate to form at least one isolation trench that adjoins said two deep trenches, said patterning using a mask comprised of a continuous lines and spaces pattern such that at least one active area is defined by said isolation trench and by said two deep trenches, said active area including said buried strap region, each of said lines and said spaces extending across an entire length said memory cell array;

forming a doped region in a top surface of said semiconductor substrate adjacent to said gate dielectric layer of said at least one deep trench;

forming a contact region to said further polysilicon layer that connects said further polysilicon layer to an insulated word line;

depositing a first insulator layer atop said surface of said semiconductor substrate;

planarizing said first insulator layer to said top surface of said insulated word line;

depositing a further insulator layer atop said first insulator layer and atop said insulated word line;

patterning and etching said further insulator layer and said first insulator layer to form at least one first opening therein that extends down to said first terminal, a remaining portion of said first insulator layer covering said further side of said deep trench;

patterning and etching said further insulator layer to form at least one further opening therein that extends from a top surface of said further insulator layer down to said first opening and that leaves a region of said further insulator layer atop said remaining portion of said first insulator layer and atop at least part of said insulated word line; and

filling said first opening and said further opening with a conducting material to form a bit line contact.

44. A memory cell for a memory cell array; said memory cell comprising:

at least two deep trenches formed within a semiconductor substrate;

a buried plate region adjoining a bottom region of at least one of said two deep trenches within said semiconductor substrate;

a dielectric film formed along the sidewalls of said at least one deep trench, an upper region of a portion of said dielectric film being removed such that a trench collar is formed along an upper portion of a side of said at least one deep trench, said portion of said dielectric film being defined by a patterned masking layer such that a further portion of said dielectric film is covered by said masking layer and said portion of said dielectric film is exposed;

said at least one deep trench being at least partly filled with doped polysilicon, the dopants in the polysilicon diffusing through said side of said at least one deep trench into an adjoining region of said semiconductor substrate to form a buried strap region along said side of said at least one deep trench;

a trench top oxide layer formed atop said doped polysilicon;

a gate dielectric layer formed on said upper portion of said side of said at least one deep trench;

said at least one deep trench being filled with a further polysilicon layer atop said trench top oxide layer;

at least one isolation trench adjoining said two deep trenches, said one isolation trench being defined using a mask comprised of a lines and spaces pattern such that at least one active area is defined by said isolation trench and by said two deep trenches, said active area including said buried strap region, each of said lines and said spaces extending across said memory cell array;

a doped region formed in a top surface of said semiconductor substrate adjacent to said gate dielectric layer of said at least one deep trench;

a contact region to said further polysilicon layer that connects said further polysilicon layer to an insulated word line;

a first insulator layer disposed atop said surface of said semiconductor substrate, said first insulator layer having a top surface substantially coplanar with a top surface of said insulated word line;

a further insulator layer disposed atop said first insulator layer and atop said insulated word line;

at least one first opening being formed in said further insulator layer and said first insulator layer that extends from within said further insulator layer through said first insulator layer down to said first terminal, a remaining portion of said first insulator layer covering said further side of said deep trench;

at least one further opening being formed within said further insulator layer from a top surface of said further insulator layer to said first opening, a region of said further insulator layer remaining atop said remaining portion of said first insulator layer and at least part of said insulated word line structure; and

a conducting material filling said first opening and said further opening to form a bit line contact.